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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,780	02/18/2004	Koichi Morikawa	031794-12	1107

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EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,780	MORIKAWA, KOICHI	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3* is/are rejected.

7)☒ Claim(s) *2 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02-18-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Information Disclosure Statement, IDS, filed February 18, 2004 has been considered by the Examiner.

2. Claims 1 – 4 are pending.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Lewallen et al. (US Pat 4,764,899).

Regarding **claims 1 and 3**, Lewallen et al. disclose a multi-port semiconductor memory device (figs. 1 – 3) comprising:

a memory cell array including a plurality of memory cells (fig. 1, array X core cells with an exemplary cell 1);

a first bit line pair performing write-in or read-out of complementary data for the memory cells in the memory cell array (fig. 1, bit line pair BL1 and BL2 coupled to left port read-write circuit 27);

a second bit line pair performing write-in or read-out of complementary data for the memory cells in the memory cell array (fig. 1, bit line pair BR1 and BR2 coupled to the right port read-write circuit 33);

a plurality of first word lines provided for each of the memory cells for selecting the memory cell that is accessed to the first bit line pair from the memory cell array (fig. 1, exemplary word line 19 is one of the plurality of same in X core cells);

a plurality of second word lines provided for each of the memory cells for selecting the memory cell that is accessed to the second bit line pair from the memory cell array (fig. 1, exemplary word line 21 is one of the plurality of same in X core cells);

a first pull-up circuit (fig. 1, FETs 41 and 43) that pulls up a low-level side of the concerned first bit line pair (col. 4, lines 27 – 37, the bit lines BL1 and BL2 are driven high to nearly logic 1 of about 5 Volts) when data is written in the memory cell that is selected from the first bit line pair (col. 4, lines 37 – 41, "Leakers 39 – 45 are capable of supplying enough current to overcome normal losses of voltage on the bit-lines due to diode leakage, but are not sufficient to raise the voltage on these lines from 0 to 1 in the event that a turned-on transistor is pulling them down to 0—logic low written to a bit line." This corresponds to applicant's specification when logic low is written to bit line BLA to cause it to go low, i.e. 0.9V, even during when pull-up transistors 161 and 162 are on and power line VDD is applied to the port A bit lines BLA, /BLA. See specification page 10, second paragraph.); and

a second pull-up circuit (fig. 1, FETs 39 and 45) that pulls up a low-level side of the concerned second bit line pair when data is written in the memory cell that is

selected from the second bit line pair (see above for similar discussion on leakers 39 and 45).

Allowable Subject Matter

5. **Claims 2 and 4** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

The prior arts teach the multi-port semiconductor memory as described in claims 1 and 3, except further comprising:

a first regulator circuit and a second regulator circuit that regulate lower power potential of the memory cell such that the low-level for the first bit line pair and the low-level of the second bit line pair, respectively, after pull-up is written in the memory cell as low-level.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly D Pham
October 15, 2005

V. Nguyen

VIET Q. NGUYEN
PRIMARY EXAMINER